#26 Appeal Brief
M. Brunson
8/28/02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of:	Anthony *et al.*	Docket:	TI-24953
Serial No.:	09/116,138	Examiner:	A. Mai
Filed:	07/15/98	Art Unit:	2814
For:	High Permittivity Silicate Gate Dielectric		

APPEAL BRIEF TRANSMITTAL FORM

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David Denker Reg. No. 40,987

August 15, 2002

Assistant Commissioner of Patents
Washington, D.C. 20231

Dear Sir:

Transmitted herewith in triplicate is an Appeal Brief in the above-identified application.

Please charge any required fee for filing the Brief—including needed extension of time fees—to the deposit account of Texas Instruments Incorporated, Account No. 20-0668. **Two additional copies of this sheet are enclosed.**

Respectfully submitted,

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APPEAL BRIEF

Applicants' Appeal Brief is submitted pursuant to 37 C.F.R. §1.192 and subsequent to a Notice of Appeal mailed April 15, 2002.

Applicants appeal the Examiner's rejection dated January 14, 2002, rejecting claim 1. Applicants provisionally appeal the rejection dated May 9, 2001 rejecting claims 2 - 9, 12 - 15, 24, 25, and 36 - 40.

Real Party In Interest:

This application is assigned to Texas Instruments Incorporated.

Related Appeals And Interferences:

There are no related appeals or interferences.

Status of the Claims on Appeal

Claims 1-30, 36-40 and 46-80 are pending. Claims 1, 26, 27, and 30 are currently active.

- Claim 1 has been rejected.
- Claims 26, 27, and 30 were found to have allowable subject matter, but are objected to.

Claims 2 - 25, 28, 29, 36 - 40, and 46 - 80 are currently withdrawn from consideration. Applicants elected to pursue Group I, Species Ie-1-3: Claim 30. Applicants traversed the restriction

requirement, but Examiner deemed the requirement proper. Applicants have petitioned the Commissioner under 37 C.F.R. § 1.144 to reverse the restriction requirement. Applicants have not yet received a ruling on the petition. Of these claims:

- Claims 2 - 9, 12 - 15, 24, 25, and 36 - 40 were rejected on 5/9/01.
- Claims 10, 11, 16 - 23, 28, and 29 were found to have allowable subject matter, but were objected to on 5/9/01.
- Claims 46 - 80 have not yet been examined.

As Applicants do not know how the petition will be decided, Applicants will submit provisional arguments addressing the possibility that the restricted claims are active.

Status of Amendments Filed After Final Rejection

Applicants filed an amendment after the final rejection to add Fig. 21 to the drawings. That amendment did not change the claims. Applicants have not received confirmation that Examiner considered the amendment.

Summary of the Invention

This invention relates generally to semiconductor device structures and methods for forming such, and more specifically to such structures and methods related to gate dielectrics for field effect devices formed on integrated circuits. [1:12][1]

As devices have scaled to smaller and smaller dimensions, the gate dielectric thickness has continued to shrink. Although further scaling of devices is still possible, scaling of the gate dielectric thickness has almost reached its practical limit with the conventional gate dielectric material, silicon dioxide. [3:5 - 3:9].

Realizing the limitations of silicon dioxide, researchers have searched for alternative dielectric materials which can be formed in a thicker layer than silicon dioxide and yet still produce the same field effect performance. This performance is often expressed as "equivalent

[1] [1:12] denotes page 1, line 12.

oxide thickness": although the alternative material layer may be thick, it has the equivalent effect of a much thinner layer of silicon dioxide (commonly called simply "oxide"). Many, if not most, of the attractive alternatives for achieving low equivalent oxide thicknesses are metal oxides, such as tantalum pentoxide and barium strontium titanate. [3:20 - 4:5].

Researchers have found formation of such metal oxides as gate dielectrics to be problematic. At typical metal oxide deposition temperatures, the oxygen ambient or oxygen-containing precursor required to form them tends to also oxidize the silicon substrate, producing an oxide layer at the interface between the substrate and the gate dielectric. The presence of this interfacial oxide layer increases the effective oxide thickness, reducing the effectiveness of the alternative gate dielectric approach. The existence of the interfacial oxide layer places an ultimate constraint on the performance of an alternative dielectric field effect device. [4:6 - 4:16].

The present invention generally avoids the problems of other alternative dielectrics by employing an oxidized dielectric material comprising a significant amount of silicon, particularly at the silicon/dielectric interface. In one preferred embodiment, a graded silicate layer is formed, such that near the silicon interface the silicate layer has a large SiO_2 component, while the upper portion of the silicate layer has a large metal oxide component. Such a structure employs primarily SiO_2 bonding at the silicon interface, with resulting low interface state densities. However, the high atomic number metal included in the silicate layer can significantly increase the dielectric constant of the film. The present invention also provides for amorphous silicate gate dielectrics, which have dense microstructures and avoid many of the problems associated with grain boundaries in polycrystalline dielectrics. [5:6 - 5:20].

In one aspect of the invention, a method of fabricating a semiconductor device is disclosed that comprises providing a single-crystal silicon substrate, forming a metal silicate dielectric layer on the substrate, and forming a conductive gate overlying the metal silicate dielectric layer. [5:21 - 5:25].

A field effect semiconductor device comprising a high permittivity silicate gate dielectric and a method of forming the same are disclosed herein. The device comprises a silicon substrate **20** having a semiconducting channel region **24** formed therein. A metal silicate gate dielectric layer **36** is formed over this substrate, followed by a conductive gate **38**. Silicate layer **36** may

be, e.g., hafnium silicate, such that the dielectric constant of the gate dielectric is significantly higher than the dielectric constant of silicon dioxide. However, the silicate gate dielectric may also be designed to have the advantages of silicon dioxide, e.g. high breakdown, low interface state density, and high stability. The present invention includes methods for depositing both amorphous and polycrystalline silicate layers, as well as graded composition silicate layers. [39:3 - 39:17].

Issues Presented for Review

1. Whether claim 1 is clearly anticipated under 35 U.S.C. § 102(b) by the Hsieh *et al.* patent (Hsieh '035).

2. Whether claim 1 is clearly anticipated under 35 U.S.C. § 102(e) by the Thakur *et al.* (Thakur '748).

Provisional Issues

P3. Whether claims 3 and 13 are enabled as required by 35 U.S.C. § 112, first paragraph.

P4. Whether claims 4 - 7 are indefinite under 35 U.S.C. § 112, second paragraph.

P5. Whether claims 36 - 40 are clearly anticipated under 35 U.S.C. § 102(b) by Hsieh '035.

P6. Whether claims 2 and 3 are clearly anticipated under 35 U.S.C. § 102(e) by Thakur '748.

P7. Whether claim 2 is rendered obvious under 35 U.S.C. § 103 by Hsieh '035, in view of WOLF, VOL. 1.

P8. Whether claims 4 - 7 are rendered obvious under 35 U.S.C. § 103 by Thakur '748, in view of the Leas patent (Leas '615).

P9. Whether claims 8, 9, and 12 - 15 are rendered obvious under 35 U.S.C. § 103 by Thakur '748, in view of the Hasegawa patent (Hasegawa '015).

P10. Whether claims 24 and 25 are rendered obvious under 35 U.S.C. § 103 by Hsieh '035.

Grouping of Claims

Claims 1 stands independently—as the only active, rejected claim.

Provisional grouping

Claims 2, and 4 - 9, and 12 - 15 stand and fall together. Claims 36 - 40 stand and fall together. Claims 24 and 25 stand and fall together. Claim 3 stands independently.

Status of the Claims on Appeal

Claims 1-30, 36-40 and 46-80 are pending. Claims 1, 26, 27, and 30 are currently active.

- Claim 1 has been rejected.
- Claims 26, 27, and 30 were found to have allowable subject matter, but are objected to.

Claims 2 - 25, 28, 29, 36 - 40, and 46 - 80 are currently withdrawn from consideration. Applicants elected to pursue Group I, Species Ie-1-3: Claim 30. Applicants traversed the restriction requirement and have petitioned the Commissioner under 37 C.F.R. § 1.144 to reverse the restriction requirement. Applicants have not yet received a ruling on the petition. Of these claims:

- Claims 2 - 9, 12 - 15, 24, 25, and 36 - 40 were rejected on 5/9/01.
- Claims 10, 11, 16 - 23, 28, and 29 were found to have allowable subject matter, but were objected to on 5/9/01.
- Claims 46 - 80 have not yet been examined.

Arguments

1. Hsieh '035 does not anticipate claim 1.

Claim 1 is limited to methods of "**fabricating a field-effect device** on an integrated circuit, comprising the steps of: providing a single-crystal silicon substrate; forming a metal silicate

dielectric layer on the substrate; and **forming a conductive gate** overlying the metal silicate dielectric layer."

The office action notes that that Hsieh '035 fabricates a Metal Oxide Semiconductor (MOS) structure. The Office Action then argues that "a MOS device is well known in the semiconductor art to be a field-effect device."[2] Although Applicants understand that the well-known MOSFET is a field-effect device, Applicants disagree that all MOS devices are field-effect devices. If Examiner persists in this assertion, Applicants request that Examiner provide suitable citations to establish this assertion.

A. Beyond the unsupported assertion discussed directly above, the office action does not show that Hsieh '035 fabricates a field-effect device.[3] In reality, Hsieh '035 is directed to "This invention relates to a method of fabricating high dielectric constant insulators, particularly a dielectric material having a high quality index for use in the integrated semiconductor circuit technology, and to capacitors using same."[4]

B. Additionally, the office action alleges that Hsieh '035 teaches "forming a conducting gate 14 overlying the metal silicate dielectric layer". Applicants agree that conductive layer 14 is deposited on the Ta_2O_5 / SiO_2 mixture layer 12'. However, Hsieh '035 states that layer 14 is a capacitor electrode[5]—not a conductive gate[6] of a field-effect device.

Since Hsieh '035 does not show "each and every element claimed[7]", a rejection under 35 U.S.C. 102 is improper. Applicants request allowance of claim 1 and its dependents.

2. Thakur '748 does not anticipate claim 1.

Claim 1 is limited to methods of "**fabricating a field-effect device** on an integrated circuit, comprising the steps of: providing a single-crystal silicon substrate; forming a metal silicate

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[2] See the January 14, 2002 Office Action at page 5, para. 7.
[3] Beyond the argument given in the January 14, 2002 Office Action at page 5, para. 7.
[4] Hsieh '035, [1:8].
[5] Hsieh '035, [3:15] ("A conductive layer 14 made of, e.g., doped polysilicon, a metallic silicide or a metal, is deposited on the oxide mixture layer 12' to form a capacitor having electrodes or plates 10 and 14 with the dielectric medium 12'.").
[6] Gate: "**3.** One of the electrodes in a field-effect transistor." MCGRAW HILL DICTIONARY OF SCIENTIFIC AND TECHNICAL TERMS 833 (5th Ed. 1994).

dielectric layer on the substrate; and **forming a conductive gate** overlying the metal silicate dielectric layer."

C. The office action asserts that Thakur '748 teaches "forming a conducting gate (66) overlying the metal silicate dielectric layer (See Fig. 7)." Applicants agree that conductive layer 66 is deposited on the $TiO_xSi_yO_z$ dielectric 65. However, Thakur '748 states that—for his capacitor of Fig. 7—"bottom electrode 64 mak[es] contact to an underlying diffusion region 61".[8] Ordinary artisans understand that a conductive gate would directly overly a gate dielectric AND a channel region. Thus, ordinary artisans understand that Thakur '748 teaches a capacitor electrode, not a conductive gate of a field-effect device.

Since Thakur '748 does not show "each and every element claimed", a rejection under 35 U.S.C. 102 is improper. Applicants request allowance of claim 1 and its dependents.

Provisional Arguments

P3. The specification enables claims 3 and 13.

D. The specification provides clear guidance to ordinary artisans about how to make the inventions of claims 3 and 13—which are both limited to methods where the Si surface has been oxidized before depositing a metal on the silicon. The office action notes that refractory metals do not enter into significant reactions with silicon oxide. This may well be true for thick layers of silicon oxide. However, the office action has not shown that this is true for very thin layers of silicon oxide. With very thin layers, the metal may often react with the underlying silicon, as the silicon oxide layer is too thin to serve as an effective reaction barrier. As a case in point, Gardner *et al.*'s 5,851,921 patent[9] (Gardner '921) discusses how artisans should avoid oxide layers above 50 angstroms when forming silicides with group VIII metals.[10] This implies that ordinary artisans might expect substantially thinner layers to have different behavior. This application clearly

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[7] The CAFC reiterated in Leinoff, 726 F.2d 734, 220 U.S.P.Q. 845 (Fed. Cir., 1984), that "to anticipate a claim, a prior art reference must show each and every element claimed."
[8] Thakur '748, [3:8].
[9] Gardner '921 was cited in a previous rejection.
[10] Gardner '921, [2:25].

teaches how ordinary artisans can use thin silicon oxide layers as a base layer for the metal silicate dielectric.[11]

Thus, Applicants submit that the specification enables ordinary artisans to make and use the invention of claims 3 and 13.

P4. Claims 4 - 7, and 9 are clear and definite.

E. In the August 2001 amendment, Applicants amended claim 4 to remove the term "both".

F. Claim 6—and thus its dependent, claim 7—is limited to methods where "the reducing gas is selected from the group consisting of CO, H2, CH3, and combinations thereof." Since parent claim 4 recites "a reducing gas", Applicants believe that this claim has sufficient antecedent basis.

G. Claim 9 refers to "the oxygen plasma". Since parent claim 4 recites "an oxygen plasma", Applicants believe that this claim has sufficient antecedent basis.

P5. Claims 36 - 40 are not anticipated by Hsieh '035.

H. The arguments in favor of claim 1 are repeated by reference because they also show that Hsieh '035 does not teach the device made by the method of claim 1—or its dependants 2, 12, 16, 24, or 26. Since Hsieh '035 does not show "each and every element claimed", a rejection under 35 U.S.C. 102 is improper. Applicants request allowance of claims 36 - 40.

P6. Thakur '748 does not anticipate claims 2 or 3.

I. The arguments in favor of parent claim 1 are repeated by reference. Since Thakur '748 does not show "each and every element claimed", a rejection under 35 U.S.C. 102 is improper.

J. Claim 3 also includes the limitation of "oxidizing less than 1 nanometer of the clean Si surface prior to the depositing a first metal step." Instead of teaching oxidizing less than 1 nm of

[11] See, e.g., Application, [8:21], [12:4], [18:1], and [21;12].

the clean Si surface, Thakur '748 teaches "...the surface of a silicon substrate 10 is pre-cleaned to remove impurities 11 which typically will be or include native oxide 4."[12]

Applicants request allowance of claims 2, 3, and their dependents.

P7. Hsieh '035 and WOLF, VOL. 1 do not render claim 2 obvious.

Applicants respectfully traverse examiner's interpretation of the prior art as rendering the invention obvious over this patent.

K. First, in regards to Hsieh '035, not only does Hsieh '035 not teach Applicants' invention of claim 2, it fails to suggest forming a metal silicate gate dielectric in a field-effect device.

L. The Office Action notes that WOLF, VOL. 1 describes various methods of forming a metal silicide. Thus, it seems that WOLF, VOL. 1 is being applied only as a reference against some of Applicants' particularized variations. Applicants submit that WOLF, VOL. 1 does not cure any of the deficiencies in the rejection noted above. Applicants repeat—by reference—the arguments above in favor of claim 1.

As such, Applicants submit that claim 2—and its dependents—are patentable over the cited art, because the references—taken together—would not have suggested the invention to those of ordinary skill in the art.

P8. Thakur '748 and Leas '615 do not render claims 4 - 7 obvious.

Applicants respectfully traverse examiner's interpretation of the prior art as rendering the invention obvious over these patents.

M. First, in regards to Thakur '748, not only does Thakur '748 not teach Applicants' invention of claim 2, it fails to suggest forming a metal silicate gate dielectric in a field-effect device.

[12] Thakur '748 [2:25]; see also Thakur '748 [claim 2].

Leas '615 is non-analogous art

N. Applicants submit that ordinary artisans would not look to Leas '615 when determining suitable methods for fabricating field-effect devices on integrated circuits. According to the title, Leas '615 is concerned with "Hot Sand-Coal Cracking to Hydrodistillate Fuels". Ordinary artisans would consider this patent to be concerned principally with organic chemistry and the petroleum industry. Applicants believe that with the rich body of literature concerning silicon processing, ordinary artisans would not search organic chemistry references to determine suitable methods of forming metal silicates from metal silicides. As such, Leas '615 is non-analogous art, and should not be combined with the other references without a specific teaching or suggestion in the cited art.

Leas '615 seems to teach a reversible cycle, not formation of a layer of silicate

O. Leas '615 teaches using hot dicobalt silicide to recover both H_2 and O_2 in a dicobalt silicide to cobaltous orthosilicate to dicobalt silicide cycle within a reactor. Additionally, the dicobalt silicide is used to recover oxygen from the organic oxygenated coal oils—thus forming the cobaltous orthosilicate of the previous cycle. Leas '615 teaches that this use of the cobalt silicide reduces the amount of purchased O_2 and H_2 needed to upgrade coal.[13]

Applicants submit that—without an explicit suggestion—ordinary artisans would not look to this reversible cycle or to oxygen recovery from coal to form the claimed metal silicate dielectric layer.

Leas '615 does not cure any of the deficiencies in the rejection of the parent claims

P. Applicants submit that Leas '615 does not cure any of the deficiencies in Thakur '748. Applicants repeat—by reference—the arguments above in favor of parent claim 2.

Applicants submit that claims 4 - 7—and their dependents—are patentable over the cited art, because the references—taken together—would not have suggested the invention to those of ordinary skill in the art.

[13] Leas '615 [3:46].

P9. Thakur '748 and Hasegawa '015 do not render claims 8, 9, and 12 - 15 obvious.

Hasegawa '015 teaches away from forming a metal silicate dielectric layer

Q. First, Hasegawa '015 does not cure the deficiencies of Thakur '748.

R. Additionally, Hasegawa '015 teaches the advantages of forming a "high dielectric constant material containing tantalum expressed by chemical formula $Ta_xO_yN_z$".[14] Applicants submit that ordinary artisans would not consider $Ta_xO_yN_z$ a metal silicate dielectric. Hasegawa '015's useful high dielectric constant material can be used as "a dielectric film for a capacitor in the example above, however, it is also effective to use the film as a gate insulating film of a MOS transistor."[15] As such, it teaches directly away from Applicants' metal silicate gate dielectric. Teaching away is the antithesis of obviousness. Applicants submit that claim 1 and its dependants are patentable over the cited references because the references—taken together—do not suggest the claimed invention to one of ordinary skill in the art. Applicants therefore respectfully request allowance of independent claim 1 and its dependents.

Hasegawa '015 does not teach the specialized techniques of claim 8 or 9

Claim 8 depends upon claim 2 and is further limited to methods "wherein the oxidizing step comprises exposure of the layer of a silicide to an oxygen plasma", while claim 9 adds the further limitation to claim 8 of "wherein the oxygen plasma is exposed to ultraviolet radiation".

S. To the extent that Hasegawa '015 teaches anything about oxidizing a metal silicide, it teaches away from using an oxygen plasma. "As described above, the process for forming a high dielectric film according to a fourth embodiment of the present invention comprises subjecting a high dielectric film to a plasma treatment using a gas containing at least nitrogen, for instance, gaseous NH_3.[16] ... Accordingly, the leak current characteristics and the isolation voltage characteristics can be improved more effectively by employing the present process instead of a

[14] Hasegawa '015 [abstract].
[15] Hasegawa '015 [8:36].
[16] Hasegawa '015 [4:53].

conventional high frequency oxygen plasma treatment."[17] Thus, Hasegawa '015 teaches either nothing about or teaches away from the specialized method of claim 8.

T. In regards to claim 9, Hasegawa '015 does not seem to teach anything about exposing an oxygen plasma to UV radiation. Hasegawa '015's only reference to UV radiation refers to gaseous oxygen, not plasma.[18]

Thakur '748 teaches away from the specialized technique of claim 13.

As the 5/14/2001 Office Action notes on the middle of page 9, "the substrate of Thakur comprises a clean Si surface immediately prior to the deposition step." This is supported by Thakur '748's teaching of "the surface of a silicon substrate 10 is pre-cleaned to remove impurities 11 which typically will be or include native oxide 4"[19] As Thakur '748 cleans the native oxide before dielectric film 30 is formed over the cleaned surface,[20] the reference teaches away from the claimed approach and obviousness is not shown.

P10. Hsieh '035 does not render claims 24 and 25 obvious.

The claimed range of claims 24 and 25 are a change of type, not just a change of size

U. Claims 24 and 25 also contains additional limitations. These limitations include "the intermediate layer having a thickness less than 1 nanometer" and oxygen annealing this intermediate layer. Hsieh '035's silicide layer is between 4 and 16 nm thick[21], before it is oxidized. In contrast, Applicants claim is limited to methods where intermediate layers thinner than 1 nm are oxygen annealed. Thus, the claimed range is not a mere change in size, but at least a factor of four[22] less than Hsieh '035's teachings.

The 1/13/00 Office Action asserted that this 4:1 ratio is not an apples-to-apples thickness comparison.[23] Applicants note that the claim limitation and Hsieh '035's description both refer to

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[17] Hasegawa '015 [5:1].
[18] "and then applying an active oxygen annealing treatment (for instance, irradiating ultraviolet radiation in the presence of gaseous O_2) to the as-deposited Ta2O5 film." Hasegawa '015 [1:57].
[19] Thakur '748 [2:25]; see also Thakur '748 [claim 2].
[20] Thakur '748 [2:38].
[21] See Hsieh '035, Fig 3.
[22] (and may be more than a factor of 16).
[23] See paper 12, page 9, second dot.

the thickness before oxidation. The fact that the materials being oxidized may be different points to unobviousness—not similarity.

Hsieh '035 limits its range to between 4 nm and 16 nm. However, Hsieh '035 teaches that maximum capacitance is found at a 7 nm thickness[24], and that "the relatively low capacitance produced at 4 nanometers of silicide is due to the formation of a layer of silicon dioxide between the silicon substrate 10 and the hafnium oxide-silicon dioxide mixture layer 12. . ." Applicants have not found where Hsieh '035 teaches that using repeated applications of 1 nm intermediate layers will get around this limitation of its useful method. Instead, Applicants submit that Hsieh '035 teaches away from oxidizing thin layers. As such, Applicants invention is a change in type, not merely a change in size.

Applicants submit that Claims 24 and 25 are patentable over the cited art, because the references—taken together—would not have suggested the invention to those of ordinary skill in the art.

Conclusion

V. Hsieh '035 does not anticipate claim 1. Hsieh '035 is directed to a method of fabricating high dielectric constant insulators, not methods of fabricating a field-effect device on an integrated circuit. Hsieh '035 teaches that overlying layer 14 is a capacitor electrode —not a conductive gate of a field-effect device.

W. Thakur '748 does not anticipate claim 1. Ordinary artisans understand that Thakur '748 teaches a capacitor electrode, not a conductive gate of a field-effect device.

Provisional Arguments

X. The specification enables claims 3 and 13. The specification provides clear guidance to ordinary artisans about how to use thin silicon oxide layers as a base layer for the metal silicate dielectric.

Y. Claims 4 - 7, and 9 are clear and definite as described above.

[24] [Hsieh '035, 4:43].

Z. Claims 36 - 40 are not anticipated by Hsieh '035. The arguments in favor of claim 1 are repeated by reference.

AA. Thakur '748 does not anticipate claims 2 or 3. The arguments in favor of parent claim 1 are repeated by reference. Claim 3 also includes the limitation of "oxidizing less than 1 nanometer of the clean Si surface prior to the depositing a first metal step." Thakur '748 teaches "...the surface of a silicon substrate 10 is pre-cleaned to remove impurities 11 which typically will be or include native oxide 4."

BB. Hsieh '035 and WOLF, VOL. 1 do not render claim 2 obvious. examiner's interpretation of the prior art as rendering the invention obvious over this patent. Applicants submit that WOLF, VOL. 1 does not cure any of the deficiencies in the Hsieh '035 rejection.

CC. Thakur '748 and Leas '615 do not render claims 4 - 7 obvious. Leas '615 is non-analogous art. Leas '615 seems to teach a reversible cycle, not formation of a layer of silicate.

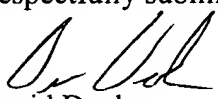
DD. Thakur '748 and Hasegawa '015 do not render claims 8, 9, and 12 - 15 obvious. Hasegawa '015 teaches away from forming a metal silicate dielectric layer. Additionally, Hasegawa '015 teaches either nothing about or teaches away from the specialized method of claim 8. Hasegawa '015's only reference to the UV radiation of claim 9 refers to gaseous oxygen, not plasma. Thakur '748 teaches away from the specialized technique of claim 13 by teaching removing the native oxide before dielectric film 30 is formed.

EE. Hsieh '035 does not render claims 24 and 25 obvious. The claimed range of claims 24 and 25 are a change of type, not just a change of size.

FF. Applicant believes that the application is in condition for allowance. However, should Examiner have any further comments or suggestions, Applicant respectfully requests that Examiner contact the undersigned in order to quickly resolve any outstanding issues.

Please charge any required fee to the deposit account of Texas Instruments Incorporated, Account No. 20-0668.

Respectfully submitted,



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APPENDIX

CLAIMS ON APPEAL

1. A method of fabricating a field-effect device on an integrated circuit, comprising the steps of:

providing a single-crystal silicon substrate;

forming a metal silicate dielectric layer on the substrate; and

forming a conductive gate overlying the metal silicate dielectric layer.

CLAIMS PROVISIONALLY ON APPEAL

2. The method of claim 1, wherein the forming a metal silicate dielectric layer step comprises:

exposing a clean Si surface on the substrate;

depositing a first metal on the Si surface;

annealing the substrate in an inert ambient, thereby forming a layer of a silicide of the first metal on the substrate;

oxidizing the layer of a silicide of the first metal, thereby forming the metal silicate dielectric layer.

3. The method of claim 2, further comprising oxidizing less than 1 nanometer of the clean Si surface prior to the depositing a first metal step.

4. (amended) The method of claim 2, wherein the oxidizing step comprises simultaneous exposure of the layer of a silicide of the first metal to an oxidizing gas and a reducing gas.

5. The method of claim 4, wherein the oxidizing gas is selected from the group consisting of O_2, H_2O, N_2O, CO_2, and combinations thereof.

6. The method of claim 4, wherein the reducing gas is selected from the group consisting of CO, H_2, CH_3, and combinations thereof.

7. The method of claim 4, wherein the oxidizing gas is selected from the group consisting of O_2, H_2O, N_2O, CO_2, and combinations thereof , and wherein the reducing gas is selected from the group consisting of CO, H_2, CH_3, and combinations thereof.

8. The method of claim 2, wherein the oxidizing step comprises exposure of the layer of a silicide to an oxygen plasma.

9. The method of claim 8, wherein the oxygen plasma is exposed to ultraviolet radiation.

12. The method of claim 1, wherein the forming a metal silicate dielectric layer step comprises:

depositing a first metal on the substrate in an oxidizing ambient, thereby forming an at least partially oxidized layer on the substrate; and

annealing the substrate in an oxidizing ambient.

13. The method of claim 12, wherein the substrate comprises an oxidized silicon surface layer immediately prior to the depositing step.

14. The method of claim 12, wherein the substrate comprises a clean Si surface immediately prior to the depositing step.

15. The method of claim 12, wherein the depositing a first metal step comprises sputtering material from a target of the first metal onto the substrate.

24. The method of claim 1, wherein the forming a metal silicate dielectric layer step comprises the repeated steps of:

evaporating an intermediate layer of material onto the substrate, the material selected from the group consisting of silicon, a first metal, and combinations thereof, the intermediate layer having a thickness less than 1 nanometer; and

annealing the substrate in an oxidizing ambient, thereby at least partially oxidizing the intermediate layer.

25. (amended) The method of claim 24, wherein a first set of one or more of the intermediate layers are silicon, and a second set of one or more of the intermediate layers comprise the first metal, the first set of layers and the second set of layers being deposited in alternating fashion.

36. An integrated circuit made by the method of claim 2 .

37. An integrated circuit made by the method of claim 12 .

38. An integrated circuit made by the method of claim 16.

39. An integrated circuit made by the method of claim 24 .

40. (amended) An integrated circuit made by the method of claim 26.